

FFF0 - FFFF Interrupt vectors			
FFF0, FFF1	Illegal opcode and ÷ by zero	A681	0000
FFF2, FFF3	SWI3	0100	EEEE
FFF4, FFF5	SWI2	0103	FEF1
FFF6, FFF7	FIRQ	010F	FEF4
FFF8, FFF9	IRQ	010C	FEF7
FFFA, FFFB	SWI	0106	FEFA
FFFC, FF FD	NMI	0109	FEFD
FFFE, FFFF	Reset	A027	8C1B

MC6809 CC register	
Bit 7	Entire register set stacked
Bit 6	FIRQ Inhibit
Bit 5	Half word flag
Bit 4	IRQ Inhibit
Bit 4	Negative flag
Bit 2	Zero flag
Bit 1	Overflow flag
Bit 0	Carey flag
Code	Meaning
andcc \$af	Enable interrupts
orcc \$50	Disable interrupts

This document lives at: https://tlindner.macmess.org/?page_id=767

CoCo Memory Map Reference

GIME Memory Map Reference

GIME-X Memory Map Reference

FF00 - FF03 PIA 1 (more information)	
FF00	DRA / DDRA
FF01	CRA
FF02	DRB / DDRB
FF03	CRB

FF20 - FF23 PIA 1 (more information)	
FF20	DRA / DDRA
FF21	CRA
FF22	DRB / DDRB
FF23	CRB

FF40 - Disk controller register ($\overline{SCS}$)		
Bit 7	Halt flag enable	
Bit 6	Drive select 3	
Bit 5	Density Flag	
	1	Double
	0	Single
Bit 4	Write pre-compensation flag enable	
Bit 3	Drive motor enable	
Bit 2	Drive select 2	
Bit 1	Drive select 1	
Bit 0	Drive select 0	

FF48 - FF4B WD1779 ($\overline{SCS}$)	
FF48	Status / Command Register
FF49	Track Register
FF4A	Sector Register
FF4B	Data Register

FF60 - FF62 X-Pad interface		
FF60	X Coordinate	
FF61	Y Coordinate	
FF62	Status register	
	Bits 7-4	Unused
	Bit 3	Pen Down
	Bit 2	Pen within 1 inch
	Bit 1	Pen in X-Margin
	Bit 0	Pen in Y-Margin

FF68 - FF6B RS232 interface (more information)	
FF68	Read/write data register
FF69	Status register
FF6A	Command Register
FF6B	Control register

FF6C - FF6F DC modem interface (more information)	
FF6C	Read/write data register
FF6D	Status register
FF6E	Command Register
FF6F	Control register

FF7A - FF7B Orchestra-90	
FF7A	Left channel
FF7B	Right channel

FF7D - FF7E Speech/sound pak		
FF7D	Data	
FF7E	Status (active low)	
	Bit 7	Busy
	Bit 6	Speaking
	Bit 5	Sounding
	Bits 4-0	Unused

FF7F Multi-pak interface	
Bits 7-6	Unused
Bits 5-4	Active CTS/CART slot
Bits 3-2	Unused
Bits 1-0	Active SCS slot

FF90 Initialization register 0 (read only)			
Bit 7	CoCo 1/2 Compatible mode		
Bit 6	MMU Enabled		
Bit 5	GIME chip IRQ enabled		
Bit 4	GIME chip FIRQ enabled		
Bit 3	RAM at FEXX is constant		
Bit 2	External SCS enable		
Bit 1-0			
	MC1	MC0	ROM mode
	0	X	16K int, 16K ext
	1	0	32K internal
	1	1	32K external

FF91 Initialization register 1 (read only)		
Bit 7	Unused	
Bit 6	Memory type	
	1	256K
	0	64K
Bit 5	Timer clock source	
	1	279.365 nsec (3.58 MHz)
	0	63.695 usec (15.7 kHz)
Bits 4-1	Unused	
Bit 0	MMU task select	
	1	Enable FFA8-FFAF
	0	Enable FFA0-FFA7

FFD6 - FFD9 CPU clock rate (write only)					
R1	R0	0-7FFF	8000-FEFF	FF00-FF1F	FF20-FFFF
0	0	0.89	0.89	0.89	0.89
0	1	0.89	1.79	0.89	1.79
1	X	1.78	1.78	1.78	1.79

Write A5 to FFD9 to set 2.86 MHz.

FFDA - FFDD Memory size (write only)																	
FFDA	M0 clear																
FFDB	M0 set																
FFDC	M1 clear																
FFDD	M1 set																
<table> <tr> <th>M1</th><th>M0</th><th>Memory size</th></tr> <tr> <td>0</td><td>0</td><td>4K</td></tr> <tr> <td>0</td><td>1</td><td>16K</td></tr> <tr> <td>1</td><td>0</td><td>32K / 64K</td></tr> <tr> <td>1</td><td>1</td><td>Not used</td></tr> </table>	M1	M0	Memory size	0	0	4K	0	1	16K	1	0	32K / 64K	1	1	Not used		
M1	M0	Memory size															
0	0	4K															
0	1	16K															
1	0	32K / 64K															
1	1	Not used															

FFDE - FFDF Memory map type (write only)																							
FFDE	TY clear																						
FFDF	TY set																						
<table> <tr> <th>TY</th><th>P1</th><th>0000-7FFF</th><th>8000-FFFF</th></tr> <tr> <td>0</td><td>0</td><td>Lower 32K RAM</td><td>ROM</td></tr> <tr> <td>0</td><td>1</td><td>Upper 32K RAM</td><td>ROM</td></tr> <tr> <td>1</td><td>0</td><td>Lower 32K RAM</td><td>Upper 32K RAM</td></tr> <tr> <td>1</td><td>1</td><td>Upper 32K RAM</td><td>Upper 32K RAM</td></tr> </table>	TY	P1	0000-7FFF	8000-FFFF	0	0	Lower 32K RAM	ROM	0	1	Upper 32K RAM	ROM	1	0	Lower 32K RAM	Upper 32K RAM	1	1	Upper 32K RAM	Upper 32K RAM			
TY	P1	0000-7FFF	8000-FFFF																				
0	0	Lower 32K RAM	ROM																				
0	1	Upper 32K RAM	ROM																				
1	0	Lower 32K RAM	Upper 32K RAM																				
1	1	Upper 32K RAM	Upper 32K RAM																				

FFE0 256 Color palette register	
FFE0	Register index

FFE1 - FFE9 Direct memory access		
FFE1	Bits 20-16 of destination address	
FFE2	Bits 15-8 of destination address	
FFE3	Bits 7-0 of destination address	
FFE4	Bits 20-16 of source address	
FFE5	Bits 15-8 of source address	
FFE6	Bits 7-0 of source address	
FFE7	Auto increment register	
	Bits 7-2	Unused
	Bit 1	Read auto increment enable
	Bit 0	Write auto increment enable
FFE8	High byte to transfer	
FFE9	Low byte to transfer	

FFEF GIME-X information byte		
Bits 7-4	Major version	
Bits 3-1	Minor version	
Bit 0	Memory Type	
	1	DDR
	0	SDR

FFC0 - FFC5 Video display mode (write only)				
FFC0	V0 clear			
FFC1	V0 set			
FFC2	V1 clear			
FFC3	V1 set			
FFC4	V2 clear			
FFC5	V2 set			
V2	V1	V0	Buffer size	Display modes
0	0	0	512	AI, SG4, SG6
0	0	1	1024	G1C, G1R
0	1	0	2048	G2C, SG8
0	1	1	1536	G2R
1	0	0	3072	G3C, SG12
1	0	1	3072	G3R
1	1	0	6144	G6R, G6C, SG24
1	1	1	Not used	

FFC6 - FFD3 Video display starting address (write only)														
FFC6	F0 clear													
FFC7	F0 set													
FFC8	F1 clear													
FFC9	F1 set													
FFCA	F2 clear													
FFCB	F2 set													
FFCC	F3 clear													
FFCD	F3 set													
FFCE	F4 clear													
FFCF	F4 set													
FFD0	F5 clear													
FFD1	F5 set													
FFD2	F6 clear													
FFD3	F6 set													
16 bit video start address:														
F6		F5	F4	F3	F2	F1	F0	0	0 0 0 0 0 0 0 0					

FFD4 - FFD5 Page number (write only)				
FFD4	P1 clear			
FFD5	P1 set			
TY	P1	0000-7FFF	8000-FFFF	
0	0	Lower 32K RAM	ROM	
0	1	Upper 32K RAM	ROM	
1	0	Lower 32K RAM	Upper 32K RAM	
1	1	Upper 32K RAM	Upper 32K RAM	

FFD6 - FFD9 CPU clock rate (write only)	
FFD6	R0 clear
FFD7	R0 set
FFD8	R1 clear
FFD9	R1 set

FF92 Interrupt request enable register (writing)	
Bit 7-6	Unused
Bit 5	Enable timer IRQ
Bit 4	Enable horizontal border IRQ
Bit 3	Enable vertical border IRQ
Bit 2	Enable serial data IRQ
Bit 1	Enable keyboard IRQ
Bit 0	Enable cartridge IRQ

FF92 Interrupt flag register (reading)	
Bit 7-6	Unused
Bit 5	Timer IRQ
Bit 4	Horizontal border IRQ
Bit 3	Vertical border IRQ
Bit 2	Serial data IRQ
Bit 1	Keyboard IRQ
Bit 0	Cartridge IRQ

FF93 Fast interrupt request enable register (writing)	
Bit 7-6	Unused
Bit 5	Enable timer FIRQ
Bit 4	Enable horizontal border FIRQ
Bit 3	Enable vertical border FIRQ
Bit 2	Enable serial data FIRQ
Bit 1	Enable keyboard FIRQ
Bit 0	Enable cartridge FIRQ

FF93 Fast interrupt flag register (reading)	
Bit 7-6	Unused
Bit 5	Timer FIRQ
Bit 4	Horizontal border FIRQ
Bit 3	Vertical border FIRQ
Bit 2	Serial data FIRQ
Bit 1	Keyboard FIRQ
Bit 0	Cartridge FIRQ

FF94 Timer register MSB (write only)	
Bit 7-4	Unused
Bit 3-0	Timer bits 11-8

FF95 Timer register LSB (write only)	
Bit 7-0	Timer bits 7-0

FF98 Video mode register (write only)		
Bit 7	Mode	
	1	Graphics
	0	Text
Bit 6	Double video bandwidth	
Bit 5	Composite color phase invert	
Bit 4	Monochrome on composite out	

FF98 Video mode register (write only)				
Bit 3	Clock frequency			
	1	50Hz video		
	0	60Hz video		
Bit 2-0 (Text)	Scan lines per row			
	0	0	X	1
	0	1	0	2
	0	1	1	8
	1	0	0	9
	1	0	1	10
	1	1	0	11
	1	1	1	∞
Bit 2-0 (Graphics)	Scan lines per row			
	0	0	X	1
	0	1	0	2
	0	1	1	7
	1	0	0	8
	1	0	1	9
	1	1	0	10
	1	1	1	∞

FF99 Video resolution register (write only)				
Bit 7	Unused			
Bits 6-5	Vertical resolution			
	0	0	192 graphic lines	24 text lines
	0	1	200 graphic lines	25 text lines
	1	0	Zero / ∞	
	1	1	225 graphic lines	28 text lines
Bits 4-2	Horizontal resolution using graphics			
	0	0	0	16 bytes per row
	0	0	1	20 bytes per row
	0	1	0	32 bytes per row
	0	1	1	40 bytes per row
	1	0	0	64 bytes per row
	1	0	1	80 bytes per row
	1	1	0	128 bytes per row
	1	1	1	160 bytes per row
	Horizontal resolution using text			
	0	X	0	32 characters per row
	0	X	1	40 characters per row
	1	X	0	64 characters per row
	1	X	1	80 characters per row

FF99 Video resolution register (write only)			
Bits 1-0	Color resolution using graphics		
	0	0	2 colors (8 pixels per byte)
	0	1	4 colors (4 pixels per byte)
	1	0	16 colors (2 pixels per byte)
	1	1	256 color mode
	Color resolution using text		
	X	0	No color attributes
	X	1	Color attributes enabled
			Text Attribute Byte
			Bit 7Flash
			Bit 6Underline
			Bits 5-3Foreground color
			Bits 2-0Background color

FF9A Border color register (write only)	
Bit 7-6	Unused
Bit 5-0	Border color

FF9B 512K bank select	
FF9B	512K bank selector

FF9C Vertical text scroll register (write only)	
Bits 7-4	Unused
Bits 3-0	Scan lines to scroll text up (0-15)

FF9D Vertical offset register MSB (write only)	
Bit 7-0	Start of video in RAM (bits 18-11)

FF9E Vertical offset register LSB (write only)	
Bit 7-0	Start of video in RAM (bits 10-3)

FF9F Horizontal offset register (write only)	
Bit 7	Force 256 bytes per row for graphics Force 128 characters per row for text
Bit 6-0	Horizontal offset address

FFA0 - FFAF MMU bank registers (lower 6 bits only)		
Task 0	Task 1	
FFA0	FFA8	Bank at 0000 - 1FFF
FFA1	FFA9	Bank at 2000 - 3FFF
FFA2	FFAA	Bank at 4000 - 5FFF
FFA3	FFAB	Bank at 6000 - 7FFF
FFA4	FFAC	Bank at 8000 - 9FFF
FFA5	FFAD	Bank at A000 - BFFF
FFA6	FFAE	Bank at C000 - DFFF
FFA7	FFAF	Bank at E000 - FFFF

FFB0 - FFBF Composite color palette registers	
FFB0 - FFBF	X X I ₁ I ₀ P ₃ P ₂ P ₁ P ₀

FFB0 - FFBF RGB color palette registers	
FFB0 - FFBF	X X R ₁ G ₁ B ₁ R ₀ G ₀ B ₀

FFB0 - FFBF RGB color palette registers	
FFB0 - FFBF	0 X R ₂ G ₂ B ₂ R ₁ G ₁ B ₁ or 1 X R ₀ G ₀ B ₀ X X X